UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,879	09/11/2003	Joseph S. Elder	MIC-05632-5D	8769

22888 7590 11/16/2006

BEVER HOFFMAN & HARMS, LLP
TRI-VALLEY OFFICE
1432 CONCANNON BLVD., BLDG. G
LIVERMORE, CA 94550

EXAMINER	
VUONG, QUOCHIEN B	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/661,879	ELDER ET AL.	
	Examiner	Art Unit	
	Quochien B. Vuong	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-45* is/are pending in the application.

4a) Of the above claim(s) *16-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-15 and 20-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/16/04*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 8-15 and 20-45 in the reply filed on 07/10/2006 is acknowledged.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 01/16/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

3. Claim 44 is objected to because of the following informalities: claim 44 ends with "," instead of ".". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 recites the limitation "the range of frequencies" in claim 15, lines 1 and 2. There is insufficient antecedent basis for this limitation in the claim.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 8-15 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3, 5 and 7-10 of U.S. Patent No. 6,167,246. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Regarding claim 8 of the present application, claim 1 of U.S. Patent No. 6,167,246 encompasses all claimed limitation including a method for operating an integrated circuit (IC), the method comprising: receiving a modulated radio frequency

(RF) signal at an input terminal of the IC; varying a local oscillator in the IC across a range of frequencies at a sweeping rate higher than a data rate of the modulated RF signal to generate a local oscillator output; mixing the local oscillator output with the modulated radio frequency signal using a mixer in the IC to generate a frequency translated signal; filtering the frequency translated signal using a filter in the IC to pass a selected range of frequencies as a modulated intermediate frequency (IF) signal; and demodulating the modulated IF signal using a demodulator in the IC to generate a data output from the modulated RF signal.

Regarding claim 9 of the present application, claim 2 of U.S. Patent No. 6,167,246 encompasses all claimed limitation including wherein the local oscillator comprises a divider, an RF oscillator, and a reference oscillator forming a phase-lock-loop (PLL), and wherein varying the local oscillator comprises: generating a reference frequency using the reference oscillator; dividing an output of the RF oscillator by a division factor provided by the divider to generate a divided frequency; dynamically altering the division factor provided by the divider; adjusting the output of the RF oscillator to cause frequency lock between the divided frequency and the reference frequency; and providing the output of the RF oscillator as the local oscillator output.

Regarding claim 10 of the present application, claim 5 of U.S. Patent No. 6,167,246 encompasses all claimed limitation including wherein generating the reference frequency comprises supplying a timing signal from a timing device to the reference oscillator, wherein the timing device is external to the IC.

Regarding claim 11 of the present application, claim 3 of U.S. Patent No. 6,167,246 encompasses all claimed limitation including wherein the local oscillator comprises a divider and an RF oscillator, and wherein varying the local oscillator comprises dynamically altering a division factor provided by the divider, the division factor being applied to a frequency provided by the RF oscillator to sweep the local oscillator output through the range of frequencies.

Regarding claim 12 of the present application, claim 7 of U.S. Patent No. 6,167,246 encompasses all claimed limitation including method for operating a radio receiver formed as a monolithic integrated circuit (IC), the method comprising: supplying a control signal to a local oscillator in the monolithic IC to select an output from the local oscillator having either a fixed frequency or a varying frequency; mixing an input radio frequency (RF) signal with the output from the local oscillator using a mixer in the monolithic IC to generate a frequency translated signal; filtering the frequency translated signal using an intermediate frequency (IF) filter in the monolithic IC to generate an IF signal; and demodulating the IF signal using a demodulator in the monolithic IC to generate a data signal.

Regarding claim 13 of the present application, claim 8 of U.S. Patent No. 6,167,246 encompasses all claimed limitation including wherein the demodulator comprises a baseband filter, and wherein demodulating the IF signal comprises: applying a first control signal to a first bandwidth selection pin of the monolithic IC to adjust a bandwidth of the baseband filter; and filtering the IF signal using the baseband filter as a lowpass filter.

Regarding claim 14 of the present application, claim 9 of U.S. Patent No. 6,167,246 encompasses all claimed limitation including wherein demodulating the IF signal further comprises applying a second control signal to a second bandwidth selection pin of the monolithic IC, wherein the first control signal and the second control signal determine the bandwidth of the baseband filter.

Regarding claim 15 of the present application, claim 10 of U.S. Patent No. 6,167,246 encompasses all claimed limitation including wherein the range of frequencies comprises a band of frequencies about 2-3% around a transmit frequency of the input RF signal.

8. Claims 20-33 and 38-45 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-5 and 12-14 of U.S. Patent No. 6,324,390. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Regarding claim 20 of the present application, claim 1 of U.S. Patent No. 6,324,390 encompasses all claimed limitation including a method for operating a radio receiver formed as a monolithic integrated circuit (IC), the method comprising: filtering an input radio frequency (RF) signal using an intermediate frequency (IF) filter circuit in an all-CMOS superheterodyne receiver in the monolithic IC to generate an IF filtered output; and demodulating the IF filtered output using an all-CMOS demodulator in the monolithic IC to generate a digital data signal.

Regarding claim 21 of the present application, claim 1 of U.S. Patent No. 6,324,390 encompasses all claimed limitation including performing logic functions on the digital data signal using a decoder in the monolithic IC to generate binary data at a data output terminal of the monolithic IC.

Regarding claim 22 of the present application, claim 2 of U.S. Patent No. 6,324,390 encompasses all claimed limitation including wherein performing logic functions on the digital data signal comprises performing a decoding operation involving a changing code scheme.

Regarding claim 23-32 of the present application, claims 5 and 12-14 of U.S. Patent No. 6,324,390 encompasses all claimed limitation.

Regarding claim 33 of the present application, claim 1 of U.S. Patent No. 6,324,390 encompasses all claimed limitation including a method for decoding a radio frequency (RF) signal, the method comprising: providing the RF signal to a monolithic integrated circuit (IC); generating a local oscillator signal using an all-CMOS local oscillator in the monolithic IC; mixing the local oscillator signal with the RF signal using an all-CMOS mixer in the monolithic IC to generate a frequency translated signal; filtering the frequency translated signal using an all-CMOS filtering circuit in the monolithic IC to generate a filtered output; and demodulating the filtered output using an all-CMOS demodulator in the monolithic IC to generate a digital data signal.

Regarding claim 38-45 of the present application, claims 1, 5 and 12-14 of U.S. Patent No. 6,324,390 encompasses all claimed limitation.

9. Claims 34-37 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 of U.S. Patent No. 6,324,390 in view of claims 1-10 of U.S. Patent No. 6,167,246.

Regarding claim 34 of the present application, claim 1 of U.S. Patent No. 6,324,390 encompasses all claimed limitation of claim 33, and claim 1 of U.S. Patent No. 6,167,246 encompasses wherein mixing the local oscillator signal with the RF signal comprises varying the local oscillator signal across a range of frequencies at a sweeping rate higher than a data rate of the RF signal.

Regarding claims 35-37 of the present application, claims 1-10 of U.S. Patent No. 6,167,246 further encompasses all the claimed limitation.

10. Claims 12-15, 20-45 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 6,662,003. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-20 of U.S. Patent No. 6,662,003 encompass all the claims limitation of claims 12-15 and 20-45 of the present application.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. (U.S. Patent Number 5,930,695) in view of Okanobu (U.S. Patent Number 5,020,147).

Regarding claim 12, Yamaguchi et al. disclose a method for radio receiver (figure 6) comprising: supplying a control signal to a local oscillator to select an output from the local oscillator having either a fixed frequency or a varying frequency; mixing an input radio frequency (RF) signal with the output from the local oscillator using a mixer to generate a frequency translated signal; filtering the frequency translated signal using an intermediate frequency (IF) filter in to generate an IF signal; and demodulating the IF signal using a demodulator to generate a data signal (column 4, lines 20-38). Although Yamaguchi et al. do not specifically disclose the radio receiver and the demodulator being formed entirely on a single monolithic integrated circuit (IC) chip. However, it is well known in the art that a radio receiver formed as a monolithic IC as taught by Okanobu (column 2, lines 53-60, and figure 4). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the IC design of the receiver of Okanobu to the receiver of Yamaguchi so that the receiver and the demodulator being formed entirely on a single monolithic IC chip for reducing cost and compact design of the receiver.

Regarding claim 15, if not inherent it would have been obvious for the method of Yamaguchi et al. and Okanobu to include a range of frequencies comprises a band of frequencies about 2-3% around a transmit frequency of the input RF signal in order for the method to operate at the transmit frequency.

Regarding claim 20, Yamaguchi et al. disclose a method for operating a radio receiver, the method comprising: filtering an input radio frequency (RF) signal using an intermediate frequency (IF) filter circuit in a superheterodyne receiver to generate an IF filtered output; and demodulating the IF filtered output using a demodulator to generate a digital data signal (column 4, lines 20-38). Although Yamaguchi et al. do not specifically disclose the radio receiver formed as a monolithic integrated circuit (IC), and superheterodyne receiver and the demodulator being all-CMOS. However, it is well known in the art that a radio receiver formed as a monolithic IC as taught by Okanobu (column 2, lines 53-60, and figure 4). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the IC design of the receiver of Okanobu to the receiver of Yamaguchi so that the receiver being formed entirely on a single monolithic IC chip for reducing cost and compact design of the receiver.

Regarding claim 21, Yamaguchi et al. disclose performing logic functions on the digital data signal using a decoder to generate binary data at a data output terminal (see figure 6; column 4, lines 20-38).

Regarding claim 24, it is obvious for the method Yamaguchi and Okanobu to include the digital data signal has a DC component, the method further comprising filtering the DC component from the digital data signal using a low pass filter that includes a capacitor that is external to the monolithic IC in order to reduce noise and improve the receiver performance (see figure 1 of Okanobu)

Regarding claim 24, Okanobu discloses controlling a gain of the all-CMOS superheterodyne receiver using an automatic gain control (AGC) circuit that monitors a magnitude of the IF filtered output (see figure 1).

Regarding claim 26, Okanobu discloses providing a bias voltage to the all-CMOS superheterodyne receiver and the all-CMOS demodulator using a bias supply circuit (figure 1).

Regarding claim 28, Okanobu discloses wherein the all-CMOS superheterodyne receiver comprises a local oscillator (LO), a mixer, and a sweep generator, and wherein filtering the input RF signal comprises: generating a varying frequency output from a local oscillator in the all-CMOS superheterodyne receiver; mixing the input RF signal with the LO output signal using a mixer in the all-CMOS superheterodyne receiver to generate a frequency translated signal; and filtering the frequency translated signal using an IF filter in the IF filter circuit (figure 1).

Regarding claim 30, Okanobu (figure 1) discloses wherein the all-CMOS demodulator comprises an amplitude modulation (AM) demodulator or an ON-OFF keyed (OOK) demodulator.

Regarding claim 31, it would be obvious for the all-CMOS superheterodyne receiver of Yamaguchi et al. and Okanobu to be configured to operate in the ISM band in order to use the receiver in that specific band.

Regarding claim 33, Yamaguchi et al. disclose a method for decoding a radio frequency (RF) signal, the method comprising: providing the RF signal to a circuit; generating a local oscillator signal using a local oscillator; mixing the local oscillator

signal with the RF signal using a mixer to generate a frequency translated signal; filtering the frequency translated signal using a filtering circuit to generate a filtered output; and demodulating the filtered output using a demodulator to generate a digital data signal (column 4, lines 20-38). Although Yamaguchi et al. do not specifically disclose the radio receiver formed as a monolithic integrated circuit (IC), and the local oscillator and the filter being all-CMOS. However, it is well known in the art that a radio receiver formed as a monolithic IC as taught by Okanobu (column 2, lines 53-60, and figure 4). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the IC design of the receiver of Okanobu to the receiver of Yamaguchi so that the receiver being formed entirely on a single monolithic IC chip for reducing cost and compact design of the receiver.

Regarding claim 38, Yamaguchi et al. disclose mixing the local oscillator signal with the RF signal comprises maintaining the local oscillator signal at a fixed frequency (column 4, lines 20-38).

Regarding claim 39, it is obvious for the method Yamaguchi and Okanobu to include filtering a DC component from the digital data signal using a low pass filter that includes a capacitor that is external to the monolithic IC in order to reduce noise and improve the receiver performance (see figure 1 of Okanobu)

Regarding claim 40, Okanobu discloses controlling a gain of the all-CMOS filtering circuit using an automatic gain control (AGC) circuit that monitors a magnitude of the filtered output (figure 1).

Regarding claim 42, Okanobu discloses wherein the all-CMOS filtering circuit comprises an intermediate frequency bandpass filter (figure 1).

Regarding claim 43, Okanobu discloses wherein the all-CMOS filtering circuit comprises a lowpass filter (figure 1).

Regarding claim 44, Okanobu discloses providing the digital data signal to a decoder within the monolithic integrated circuit (figure 1).

Regarding claim 45, Okanobu discloses providing the digital data signal to a circuit integrated within the monolithic integrated circuit, said circuit being selected from the group of an arithmetic logic unit circuit, a processor circuit, and a programmable logic circuit (figure 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quochien B. Vuong whose telephone number is (571) 272-7902. The examiner can normally be reached on M-F 9:30-18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Quochien B. Vuong
Sep. 15, 2006.

QUOCHIEN B. VUONG
PRIMARY EXAMINER